COURSE SCHEME
EXAMINATION SCHEME
ABSORPTION SCHEME
&
SYLLABUS

Of

First, Second, Third & Fourth Semester
Choice Base Credit System (CBCS)
Of
Master of Technology (M.Tech)

In

V.L.S.I.

Of

RASHTRASANT TUKDOJI MAHARAJ
NAGPUR UNIVERSITY, NAGPUR

Rashtrasant Tukdoji Maharaj Nagpur University, Nagpur
Faculty of Engineering & Technology
Course and Examination Scheme of Master of Technology
Choice Base Credit System(CBCS)

I Semester M. Tech. (VLSI)

Subject Code	Subject	Teaching Scheme			Examination Scheme								
					Theory					Practical			
		Hours per week		No. of Credits	Duration of Paper (Hrs.)	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks
		L	P			University Assessment	College Assessment			University Assessment	College Assessment		
PGVLS101T	VLSI Subsystem Design	4	-	4	3	70	30	100	50	-	-	-	-
PGVLS102T	Advanced Digital Signal Processing	4	-	4	3	70	30	100	50	-	-	-	-
PGVLS103T	VLSI Circuits	4	-	4	3	70	30	100	50	-	-	-	-
PGVLS104T	Elective-I	4	-	4	3	70	30	100	50	-	-	-	-
PGOPEN105T	Elective-II (Open)	4	-	4	3	70	30	100	50	-	-	-	-
PGVLS106P	Laboratory -I Advanced Digital Signal Processing	-	2	1	-	-	-	-	-	50	50	100	50
PGVLS107P	Laboratory -II VLSI Circuits	-	2	1	-	-	-	-	-	50	50	100	50
Total		20	4		-	350	150	500	-	100	100	200	-
Semester Total		24		22	700 Marks								

Elective-I: 1. Mixed Signal Processing [PGVLS104/1T] 2. Low Power VLSI Design [PGVLS104/2T] 3. Embedded Systems [PGVLS104/3T]
Elective-II (Open): List of Open Elective-II [PGOPEN501T] is enclosed.

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II Semester M. Tech. (VLSI)

Subject Code	Subject	Teaching Scheme			Examination Scheme								
					Theory					Practical			
		Hours per week		No. of Credits	Duration of Paper (Hrs.)	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks
		L	P			University Assessment	College Assessment			University Assessment	College Assessment		
PGVLS201T	Analog VLSI Design	4	-	4	3	70	30	100	50	-	-	-	-
PGVLS202T	VLSI Testing	4	-	4	3	70	30	100	50	-	-	-	-
PGVLS203T	Modeling of Digital System and Testing	4	-	4	3	70	30	100	50	-	-	-	-
PGVLS204T	Elective-III	4	-	4	3	70	30	100	50	-	-	-	-
PGFD205T	Foundation-I	4	-	4	3	70	30	100	50	-	-	-	-
PGVLS206P	Laboratory -I Analog VLSI Design	-	2	1	-	-	-	-	-	50	50	100	50
PGVLS207P	Laboratory -II Modeling of Digital System and Testing	-	2	1	-	-	-	-	-	50	50	100	50
Total		20	4		-	350	150	500	-	100	100	200	-
Semester Total		24		22	700 Marks								

Elective-III: 1.System on Chip [PGVLS204/1T] 2.Micro Electro Mechanical Switches (MEMS) [PGVLS204/2T] 3. High Speed Semiconductor Devices and Circuits [PGVLS204/3T]
Foundation-I: Research Methodology

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III Semester M. Tech. (VLSI)

Subject Code	Subject	Teaching Scheme			Examination Scheme								
					Theory					Practical			
		Hours per week		No. of Credits	Duration of Paper (Hrs.)	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks
		L	P			University Assessment	College Assessment			University Assessment	College Assessment		
PGOPEN301T	Elective-IV (Open)	4	-	4	3	70	30	100	50	-	-	-	-
PGFD302T	Foundation II	4	-	4	3	70	30	100	50	-	-	-	-
PGVLS303P	Project Seminar	-	8	8	-	-	-	-	-	-	200	200	100
Total		8	8		-	140	60	200	-	-	200	200	-
Semester Total		-		16	400 Marks								

Elective-IV (Open): List of Open Elective-IV [PGOPEN301T] is enclosed.
Foundation II: Project Planning and Management

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IV Semester M. Tech. (VLSI)

Subject Code	Subject	Teaching Scheme			Examination Scheme								
					Theory					Practical			
		Hours per week		No. of Credits	Duration of Paper (Hrs.)	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks	Max. Marks	Max. Marks	Total Marks	Min. Passing Marks
		L	P			University Assessment	College Assessment			University Assessment	College Assessment		
PGVLS401P	Project	-	16	16	-	-	-	-	-	400	-	400	200
Total		-	16		-	-	-	-	-	400	-	400	-
Semester Total		-		16	400 Marks								

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S.N.	Code	Semester Subject Name	New Subject Code	CBCS Subject Name
1.	IFU-01	VLSI Subsystem Design(Th)	PGVLS101T	VLSI Subsystem Design
2.	IFU-04	Advanced Digital Signal Processing(Th)	PGVLS102T	Advanced Digital Signal Processing
3.	----------	----------	PGVLS103T	VLSI Circuits *
4.	IIIFU02(1)	Mixed Signal Processing(Th)	PGVLS104T/1T	Elective-I: Mixed Signal Processing
5.	IIFU05(2)	Low Power VLSI Design	PGVLS104T/2T	Elective-I: Low Power VLSI Design
6.	IFU-05	Embedded System-I(Th)	PGVLS104T/3T	Elective-I: Embedded Systems
7.	----------	----------	PGOPEN105T	Elective-II (Open): Biomedical Systems Engineering *
8.	----------	----------	PGOPEN105T	Elective-II (Open): Soft Computing Techniques *
9.	----------	----------	PGOPEN105T	Elective-II (Open): Digital Forensics*
10.	----------	----------	PGOPEN105T	Elective-II (Open): Nano Electronics*
11.	IFU-04	Advanced Digital Signal Processing(P)	PGVLS106P	Laboratory -I Advanced Digital Signal Processing
12.	----------	----------	PGVLS107P	Laboratory -II VLSI Circuits *
13.	IFU-01	VLSI Subsystem Design(P)	----------	----------
14.	IFU-02	Modeling of Digital System -1(Th)	----------	----------
15.	IFU-02	Modeling of Digital System -1(P)	----------	----------
16.	IFU-03	Switching Theory and Automata(Th)	----------	----------
17.	IFU-05	Embedded System-I(P)	----------	----------

The students who fail to clear any subject(s) of the I Semester Old Pattern by the last chance prescribed, shall be required to clear the respective equivalent subject of I Semester(New CBCS Pattern) along with the additional subject marked with (*). The Theory and Practical College and University Assessment Marks of Old Pattern will be converted into the same proportion in New CBCS Pattern. The College Assessment Marks of the Additional Theory/Practical Subject marked with (*) will be taken in same proportion of the average College Assessment Marks in all the Theory/Practical subject of old pattern.

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II Semester M. Tech. (VLSI)

S.N.	Code	Semester Subject Name	New Subject Code	CBCS Subject Name
1.	IIFU01	Analog VLSI Design(Th)	PGVLS201T	Analog VLSI Design
2.	IIIFU01	VLSI Testing(Th)	PGVLS202T	VLSI Testing
3.	IIFU02	Modeling of Digital System-II(Th)	PGVLS203T	Modeling of Digital System and Testing
4.	----------	----------	PGVLS204T/1T	Elective-III: System on Chip *
5.	----------	----------	PGVLS204T/2T	Elective-III: Micro Electro Mechanical Switches (MEMS) *
6.	----------	----------	PGVLS204T/3T	Elective-III: High Speed Semiconductor Devices and Circuits *
7.	----------	----------	PGFD205T	Foundation-I: Research Methodology*
8.	IIFU01	Analog VLSI Design(P)	PGVLS206P	Laboratory -I Analog VLSI Design
9.	IIFU02	Modeling of Digital System-II(P)	PGVLS207P	Laboratory -II Modeling of Digital System and Testing
10.	IIFU03	VLSI Signal Processing(Th)	----------	----------
11.	IIFU04	Digital Image Processing(Th)	----------	----------
12.	IIFU04	Digital Image Processing(P)	----------	----------
13.	IIFU05(1)	Advanced Computer Architecture(Th)	----------	----------
14.	IIFU05(3)	Embedded System-II	----------	----------

The students who fail to clear any subject(s) of the II Semester Old Pattern by the last chance prescribed, shall be required to clear the respective equivalent subject of II Semester(New CBCS Pattern) along with the additional subject marked with (*). The Theory and Practical College and University Assessment Marks of Old Pattern will be converted into the same proportion in New CBCS Pattern. The College Assessment Marks of the Additional Theory/Practical Subject marked with (*) will be taken in same proportion of the average College Assessment Marks in all the Theory/Practical subject of old pattern.

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III Semester M. Tech. (VLSI)

S.N.	Code	Semester Subject Name	New Subject Code	CBCS Subject Name
1.	----------	----------	PGOPEN301T	Elective-IV (Open): Wireless Sensor Network *
2.	----------	----------	PGOPEN301T	Elective-IV (Open): Bio-Informatics *
3.	----------	----------	PGOPEN301T	Elective-IV (Open): Artificial Intelligence and Robotics *
4.	----------	----------	PGFD302T	Foundation II: Project Planning and Management*
5.	IIIFU03	Project Seminar	PGVLS303P	Project Seminar
6.	IIIFU02(2)	Computer Communication Networks(Th)	----------	----------
7.	IIIFU02(3)	Computer Graphics(Th)	----------	----------

The students who fail to clear any subject(s) of the III Semester Old Pattern by the last chance prescribed, shall be required to clear the respective equivalent subject of III Semester(New CBCS Pattern) along with the additional subject marked with (*). The Theory and Practical College and University Assessment Marks of Old Pattern will be converted into the same proportion in New CBCS Pattern. The College Assessment Marks of the Additional Theory/Practical Subject marked with (*) will be taken in same proportion of the average College Assessment Marks in all the Theory/Practical subject of old pattern.

R.T.M. Nagpur University
Scheme of Examination for
M. Tech. (VLSI) First Semester

PGVLS101T	VLSI Subsystem Design

Course Objectives:

1. To study the fundamentals of MOS devices and their characteristics.
2. To lay good foundation on the design and analysis of CMOS analog integrated circuits.
3. To study Transient Optimization techniques.
4. To learn and understand clocking strategies.

Course Outcome: By the end of the course, the students shall be able to

1. Design different CMOS based circuits.
2. Analyze the model parameters of CMOS based circuits.

UNIT I: Electrical Properties of MOS Transistors (9)

Electrical Properties, Junction Diode, MOS Transistor: Operation Modes: Threshold Voltage: Metal and Polysilicon; Trapped Charge; Implants, Strong Inversion: Charge Modeling; Constant Vt model: NMOS/PMOS transistors: I/V characteristics, Parasitic Bipolar Transistors: CMOS Latch-up, Analysis (D.C. and Transient).

UNIT II: (9)

Device Capacitances and Charge Storage in MOS: NMOS/CMOS circuit analysis, Small signal amplifier model; Miller Effect, Layout / Fabrication, Diffusion / Implants / Wires, NMOS/CMOS processes, SCMOS Design Rules - special derivation; self-aligned processes, Logic Level Design, Realization of Duals for CMOS, Euler path layout, Topological Considerations.

UNIT III: (8)

Don't Cares and Redundancy, Layout Parasitic Reduction, I/V for MOS Logic Families, Prop. Delay for CMOS/NMOS/PNMOS, Layout Capacitance/Resistance Estimation; Gain effects; MOS Performance Estimation, Buffers/Capacitive Loading, Power Dissipation.

UNIT IV: (9)

Transient Optimization, Sidewall/2-d and 3-d effects: Cross-talk, Fringing, Ball-Park numbers for process Estimation: Scaling CMOS Design Optimization: High-Speed Logic Strategies, Interconnection, Distributed R/C, Cross-Talk, Noise

UNIT V: (9)

Clocking Strategies, Sub-System Design and Partitioning Dynamic Logic, Dynamic Circuits, Stored Charge and timing, Domino Logic, Switched Capacitor and Charge Flow Circuits, Pass-Transistor Logic (CPL) Data-Path and Memory Circuits: Static/Dynamic Memories, Ancillary Memory Analog Circuits.

TEXT BOOKS:

1. Weste, "Principles of CMOS VLSI Design(2nd Edition)
2. Douglas A.Pucknell and Kamran Eshraghian, "Basic VLSI Systems and Circuits", Prentice Hall of India , 1993
3. Wayne Wolf,"Modern VLSI Desin" 2nd Edition, Prentice Hall 1998

REFERENCE BOOK:

1. Sung-Mo-Kang, Yusuf Labelbici,"CMOS Digital Integrated Circuits" 3rd Ed, Mc Graw Hill

PGVLS102T	Advanced Digital Signal Processing

Course Objectives:

1. To study the basic concepts of digital signal processing.
2. To study analysis and processing of signals for different kind of applications and retrieval of information from signals.
3. To study designing of digital filters and its realization.
4. To study analysis of signals using the discrete Fourier transform (DFT) and Z-Transform.
5. To Study Power Spectrum Estimation.
6. To study the application of Wavelet Transforms.

Course Outcome: By the end of the course the students shall be able to:

1. Represent discrete-time signals analytically and visualize them in the time domain.
2. Meet the requirement of theoretical and practical aspects of DSP with regard to sampling and reconstruction.
3. Design and implement digital filter for various applications.
4. Estimation of Power Spectrum
5. Describe the concept of multi rate signal processing and how to apply it for the wavelet transform.
6. Describe the various transforms for analysis of signals and systems.

UNIT I: Multirate Digital Signal Processing: (9)

Introduction, Decimation by a Factor D, Interpolation by a Factor I, Sampling Rate Conversion by a Rational Factor I/D, Filter Design and Implementation for sampling rate Conversion Multirate Digital Signal Processing Multistage, Implementation of Sampling Rate Conversion, Applications of Multirate Signal Processing, Sampling Rate Conversion of Bandpass Signals Linear Prediction and Optimum Linear

UNIT II: Filters: (8)

Innovations Representation of a Stationary Random Process, Forward and Backward Linear Prediction, Solution of the Normal Equations, Properties of linear prediction - Error Filter, AR Lattice and ARMA Lattice-Ladder Filters.

UNIT III: Power Spectral Estimation: (9)

Estimation of Spectra from Finite Duration Observations of a signal, the Periodogram, Use DFT in power Spectral Estimation, Bartlett, Welch and Blackman, Tukey Methods, Comparison of performance of Non-Parametric Power Spectrum Estimation Methods

UNIT IV: Parametric Method of Power Spectrum Estimation: (10)

Parametric Methods for power spectrum estimation, Relationship between Auto-Correlation and Model Parameters, AR (Auto-Regressive) Process and Linear Prediction, Yule-Walker, Burg and Unconstrained Least Squares Methods, Sequential Estimation, Moving Average(MA) and ARMA Models Minimum Variance Method, Piscaranko's Harmonic Decomposition Methods, MUSIC Method.

UNIT V: (8)

Window Selection, Wavelet Transform, STFT to Wavelet conversion, Basic Wavelet, Discrete time orthogonal Wavelet, Continuous Time Orthogonal Wavelets

TEXT BOOKS:

1. Proakis JG and Manolakis DG Digital Signal Processing Principles, Algorithms and Application, PHI.
2. Openheim AV & Schafer RW, Discrete Time Signal Processing PHI.

REFERENCE BOOKS:

1. Samuel D Stearns, "Digital Signal Processing with examples in Matlab. " CRC Press.
2. ES Gopi. "Algorithm collections for Digital Signal Processing Applications using Matlab", Springer.
3. Taan S.Elali, "Discrete Systems and Digital Signal Processing with Matlab, " CRC Press,2005.

PGVLS103T	VLSI Circuits

Course Objectives:

1. To study basics of VLSI Design methodologies.
2. To study different VLSI design rules.
3. To study in depth the flow of VLSI System Design.
4. To study VLSI Design Modeling and it's synthesis.

Course Outcome: By the end of the course, the students shall be able to

1. Describe and formulate the flow of VLSI Design for any application.
2. Simulate and Analyze the VLSI Circuits.

UNIT I: VLSI Design Methodologies (9)

Introduction to VLSI Design Methodologies – Review of Data Structures and algorithms - Review of VLSI Design Automation tools – Algorithmic Graph Theory and Computational Complexity – Tractable and Intractable problems – General Purpose methods for combinatorial optimization.

UNIT II: Design Rules (9)

Layout Compaction – Design Rules – Problem Formulation – Algorithms for constraint graph compaction – placement and partitioning – Circuit representation – Placement algorithms - partitioning

UNIT III: Floor Planning (8)

Floor planning concepts – shape functions and floor plan sizing – Types of local routing problems – Area Routing – Channel Routing – Global Routing – Algorithm for Global Routing.

UNIT IV: Simulation (9)

Simulation – Gate-Level modeling and simulation – Switch-level modeling and simulation – Combinational Logic Synthesis – Binary Decision Diagrams – Two Level Logic Synthesis.

Unit V: Modeling and Synthesis (9)

High Level Synthesis – Hardware models – Internal representation – Allocation – assignment and scheduling – Simple Scheduling algorithm – Assignment problem – High level transformations.

Text Books:

1. S. H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N. A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.

References Books:

1. Sadiq M. Sait, Habib Youssef, " VLSI Physical Design Automation: Theory and Practice", World Scientific 1999.
2. Steven M. Rubin, " Computer Aids for VLSI Design", Addison Wesley Publishing 1987.

Elective-I (Discipline Specific):

PGVLS104/1T	Mixed Signal Processing

Course Objectives:

1. To study different aspects of analog and mixed signals.
2. To study different types of ADCs and DACs.
3. To study simulation of mixed signals through VHDL and Verilog.

Course Outcome: By the end of the course, the students shall be able to

1. Describe the processing and analysis of mixed signals
2. Simulate the analog and mixed signals.

UNIT I: **(8)**

Analog circuit analysis, Network independent, dependent data sampled analog system loading effects, Analog and Mixed Signal Extensions To VHDL: Introduction, language design objectives, theory of differential algebraic equation the 1076.1. Language tolerance groups, conservative system

UNIT II: **(9)**

Time and simulation cycle A/D and D/A interaction, quiescent point, frequency domain modeling and examples, Analog and discrete-time signal processing, Analog integrated continuous-time and discrete-time (switched-capacitor) filters, Basics of Analog to digital converters (ADC), Basics of Digital to analog converters (DAC).

UNIT III: **(9)**

Successive approximation ADCs, Dual slope ADCs, High-speed ADCs (e.g. flash ADC, pipeline ADC and related architectures), High-resolution ADCs (e.g. delta-sigma converters), DACs, Mixed-Signal layout, Interconnects, Phase locked loops, Delay locked loops.

UNIT IV: **(9)**

Analog Extensions To Verilog: Introduction Equation construction solution, waveform filter functions, simulator, control analysis, multi-disciplinary model, Behavioral Generic model of operational amplifiers: Introduction, description of generic Opamp model structure, configuration functional specification

UNIT V: **(9)**

Auxiliary block conflict resolution, application examples, Non -Linear state space averaged modeling of 3-state –digital phase-frequency detector, Introduction model, resell table integrator AC analysis, sample application.

TEXT BOOKS:

1. Alain Vachoux Jean -Michel Berge OZ Levia “Analog and mixed signal hardware description languages (current issues in Electronic Modeiling V.10) Kluwer Academic Publisher 1997.

2. Thomas H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, 2 Edition, Cambridge University
Press, 2004.

REFERENCE BOOKS:

1. Andrzej Handkiewicz, "Mixed-Signal Systems: A Guide to CMOS CircuitsDesign".
2. E.N. Farag and M.I. Elmasry, Mixed SignalVLSI Wireless Design: Circuits & Systems, Kluwer,1999

Elective-I (Discipline Specific):

PGVLS104/2T	Low Power VLSI Design

Course Objectives:

1. To study the sources of Power Dissipation.
2. To study the concepts on different levels of power estimation and optimization techniques.
3. To study different Low Power Design Approaches.

Course Outcome: By the end of the course, the students shall be able to

1. Use mathematical methods and circuit analysis models in analysis of CMOS digital electronics circuits, including logic components and their interconnect.
2. Design and model Low Power VLSI applications.

UNIT I: Fundamentals: (9)

Need for Low Power Circuit Design, Sources of Power Dissipation, Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects, Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT II: Low-Power Design Approaches: (9)

Low-Power Design through Voltage Scaling, VTCMOS circuits, MTCMOS circuits, Architectural Level Approach, Pipelining and Parallel Processing Approaches, Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT III: Low-Voltage Low-Power Adders: (10)

Introduction, Standard Adder Cells, CMOS Adder's Architectures, Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques, Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT IV: Low-Voltage Low-Power Multipliers: (8)

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT V: Low-Voltage Low-Power Memories: (9)

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS:

1. CMOS Digital Integrated Circuits –Analysis and Design –Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.

2. Low-Voltage, Low-Power VLSI Subsystems –Kiat-Seng Yeo, Kaushik Roy, TMH Professional
Engineering.

REFERENCE BOOKS:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective –Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design –Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design –Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design –A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies –Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

Elective-I (Discipline Specific):

PGVLS104/3T	Embedded Systems

Course Objectives:

1. To study fundamentals of 8051 microcontroller, PIC-16c6x/7x and ARM-7.
2. To study interfacing of different peripherals with microcontrollers based upon the embedded application.

Course Outcome: By the end of the course, the students shall be able to

1. Program an embedded system
2. Design, implement and test an embedded system.

UNIT I: **(8)**

Introduction to controllers, 8051 controller, Block Diagram &Architecture, 8051 Instruction Set, Addressing modes & programming, 8051 Timers, Serial I/O, Interrupts programming,

UNIT II: **(10)**

Memory Interfacing, Programming, Real time interfacing with LED, LED display, LCD display Enhanced Features: Dallas HSM & Atmel Micro-controllers, Architecture enhancements, control store and external memory, scratchpad RAM enhancements, Timers, Serial I/O, Analog I/O, Voltage comparators.

UNIT III: **(9)**

RISC Controller: PIC Micro-controllers–overview; features, PIC 16c6x/7x–architecture, file selection register, Memory organization, Addressing modes, Instruction set, Programming, PIC-18 Flash Micro-controllers. STATUS, OPTION_REG, PCON registers

UNIT IV: **(9)**

Memory Organization: Program & Data Memory, Data EEPROM & Flash Program EEPROM, Interrupts, I/O ports, Timers, Capture/Compare/PWM module, Master Synchronous Serial Port module, USART, ADC.

UNIT V: **(8)**

ARM Micro-controllers overview; features, ARM 7 –architecture, Thumb, Register Model, Addressing modes, Introduction to Embedded C Programming.

TEXT BOOKS:

1. Embedded system Design ,Steve Heath, Butterworth Helneman,2008,4th
2. The 8051 Microcontroller-architecture, Programming & Applications, Kenneth J.Ayala, Penram International & Thomson Aisa,2003,2nd
3. The 8051 Microcontroller and Embedded Systems, Mazidi and McKinley, Pearson Education, 2010, 2nd Edition.

REFERENCE BOOKS:

1. Programming Embedded Systems with C and GNU Development Tools, Michael Barr,

Anthony Massa, O'Reilly publishers, 2nd Edition
2. Real Time Interfacing to ARM, Cortex-M Microcontrollers, Embedded systems, Jonathan Valvano, 5th Edition

Laboratory-I:

PGVLS106P	Advanced Digital Signal Processing

Any EIGHT practicals are to be conducted based on the syllabus of Advanced Digital Signal Processing [PGVLS102T]

Laboratory-II:

PGVLS107P	VLSI Circuits

Any EIGHT practicals are to be conducted based on the syllabus of VLSI Circuits [PGVLS103T]

R.T.M. Nagpur University
Scheme of Examination for
M. Tech. (VLSI) Second Semester

PGVLS201T	Analog VLSI Design

Course Objectives:

1. To introduce the fundamental principles of VLSI circuit design and to examine the basic building blocks of large-scale circuits.
2. To learn about Device Modeling- Various types of analog systems- CMOS amplifiers and Comparators.

Course Outcome: By the end of the course, the students shall be able to

1. Understand the concepts of analog design and to design various analog systems including data converters- CMOS amplifiers- Comparators and Switched Capacitor Circuits.

UNIT I: **(9)**

Device modeling and simulation Modeling, MOS Models Diode model, Bipolar modes BSIM Spice models, Circuit simulations using Spice, Basic Building Blocks: Switches, Current sources and sinks, Current mirrors, Voltage and current references.

UNIT II: **(9)**

Amplifiers: MOS Inverting amplifier, Cascade amplifiers, Feedback amplifiers, Differential amplifiers, Frequency response, noise performance in Diff amplifiers, Output amplifiers.

UNIT III: **(8)**

CMOS Two stage OPAMP Design, Cascade OPAMPs, Simulation and Measurement of OPAMPs, Comparators.

UNIT IV: **(9)**

Analog signal processing, CMOS Digital to analog converters, Scaling and serial, cyclic, Analog to digital converters Serial, SAR, Parallel, Pipelined, sigma-delta converters.

UNIT V: **(9)**

Mixed signal Layout issues, Continuous time filters, Switched capacitor filters, Modulator and multipliers, PLL, Advance topics on Analog VLSI.

TEXT BOOKS:

1. VLSI Design Techniques for analog and digital circuits, R.L.Geiger, P.E.Allen, McGRaw Hill, 2008, 4th Edition
2. CMOS circuit design, Layout and simulation, J.Baker, D.E.Boyce, IEEE Press, 2003, 1st Edition

REFERENCE BOOKS:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits , McGraw-Hill, 2001

PGVLS202T	VLSI Testing

Course Objectives:

1. To know about the various test Generation Algorithms and Fault Simulation Techniques.

Course Outcome: By the end of the course, the students shall be able to

1. Do testing of various Memory Modules and Combinational & sequential logic Circuits.

UNIT I: INTRODUCTION TO TESTING (9)

Faults in digital circuits, Modeling of faults, Logical Fault Models, Fault detection, Fault location, Fault dominance, Logic Simulation, Types of simulation, Delay models, Gate level Event-driven simulation.

UNIT II: TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS (9)

Test generation for combinational logic circuits, Testable combinational logic circuit design, Test generation for sequential circuits, design of testable sequential circuits.

UNIT III: DESIGN FOR TESTABILITY (8)

Design for Testability, Ad-hoc design, Generic scan based design, Classical scan based design, System level DFT approaches.

UNIT IV: SELF-TEST AND TEST ALGORITHMS (9)

Built-In Self Test, Test pattern generation for BIST, Circular BIST, BIST Architectures, Testable Memory Design, Test algorithms, Test generation for Embedded RAMs.

UNIT V: FAULT DIAGNOSIS (9)

Logic Level Diagnosis, Diagnosis by UUT reduction, Fault Diagnosis for Combinational Circuits
Self-checking design, System Level Diagnosis.

TEXT BOOKS:

1. M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
2. M.L. Bushnell and V.D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed -Signal VLSI Circuits", Kluwer Academic Publishers, 2002.

REFERENCE BOOKS:

1. P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.
2. A.L. Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice all International, 2002

PGVLS203T	Modeling of Digital System and Testing

Course Objectives:

1. To learn different styles of modeling in Verilog.
2. To Study simulation of digital circuits.
3. To study basics of FPGA and its applications.
4. To learn fundamentals of testing of logic circuits.

Course Outcome: By the end of the course, the students shall be able to

1. Simulate different combinational and sequential circuits.
2. Test different logic circuits.

UNIT I: Verilog for System Design (9)

Introduction to HDL, Behavioural, Data flow, Structural Models, Simulation Cycles, Process, Concurrent Statements, Sequential Statements, Loops, Delay Models, Sequential Circuits, FSM Coding, Library, Packages, Functions, Procedures, Operator Inference, Writing Test bench.

UNIT II: Digital Circuit Simulation (9)

Design of combinational circuit building blocks: synthesis of logic functions using multiplexers, demultiplexers, binary encoders and priority encoders, code converters, arithmetic comparison circuits, SRAM Model

Design of Sequential Circuit Building block, Flip flops, registers with enable input, design of bit counting circuit.

UNIT III: Sequential Circuit Simulation (9)

Registers and counters: shift registers, Asynchronous counters and synchronous counters, reset synchronization, UART Model, shift and add multiplier, divider, clock synchronization, clock skew, switch debouncing, Design example - bus structure.

UNIT IV: Field Programmable Gate Arrays (8)

Introduction to FPGA, Logic Block Architecture, Routing Architecture, Programmable Interconnections, Design Flow, Xilinx Spartan architecture, Xilinx Virtex Architecture, Boundary Scan, Programming FPGA's, Constraint Editor, Static Timing Analysis, One hot encoding, Hardware-software co-simulation, Bus function models, Bus Functional Model (BFM) Simulation, Case Study: Xilinx Spartan III.

UNIT V: Testing of logic circuits (9)

Testing Philosophy, Role of Testing, fault model, complexity of a test set, Detection of single Multiple Faults in Combinational Logic Circuits, techniques for testing of sequential circuits, Design for testability.

TEXT BOOKS:

1. John F. Wakerly,"Digital Design principles and practices", 3rd edition, PHI publications
2. Zainalabedin Navabi, VHDL, analysis and modeling of digital systems, McGraw-Hill.
3. Ian Grout, Digital Systems Design with FPGAs and CPLDs, Elsevier

REFERENCE BOOKS:

1. Brown, Vranesic ―Fundamentals of digital logic design with VHDL, McGraw Hill
2. Michael John Sebastian Smith, Application-Specific Integrated Circuits, Addison Wesley

Elective-III (Discipline Specific):

PGVLS204/1T	System on Chip (SoC)

Course Objectives:

1. To study and understand different Hardware and Software System Design approaches.
2. To study the fundamentals of chip designing.
3. To learn different design customization techniques.

Course Outcome: By the end of the course, the students shall be able to

1. Describe various customization techniques for chip designing.

UNIT I: Introduction to systems approach:

System architecture, components of system, Hardware /software, Processor architecture, Memory addressing, interconnects

UNIT II: Chip basics, time, area, power reconfigurability

Design tradeoffs, requirements and specifications, Cycle time, Ideal and Practical Scaling, Area time power tradeoffs in processor design, Reliability, Configurability.

UNIT-III: Processors

Introduction, Processor selection for SOC design, Basic concepts in processor architecture, Robust Processors, vector, VLIW processor, Superscalar

UNIT-IV: Interconnects, Customization and Reconfiguration

Introduction, Bus basic architecture, SOC standard buses, AMBA, core connect, Analytic bus model, contention and shared buses, effect of bus transaction and contention, Introduction to NOC,SOC customization overview, Processor customization, Reconfigurable technologies.

UNIT V: ARM SOC Architecture

ARM architecture, Assembly language instruction set, architectural support for system development, ARM CPU cores.

TEXT BOOKS:

1. Michael J.Flynn , Wayne Luk, "Computer System Design-System on Chip",Wiley Publication

REFERENCE BOOKS:

2. Steve Furber, "ARM system on Chip Architecture", Pearson Education ltd, 2nd Edition

Elective-III (Discipline Specific):

PGVLS204/2T	Micro Electro Mechanical Switches (MEMS)

Course Objectives:

1. To understand Standard microfabrication techniques and the issues surrounding them.
2. To understand Major classes, components, and applications of MEMS devices/systems and to demonstrate an understanding of the fundamental principles behind the operation of these devices/systems
3. To understand microfabrication techniques and applications to the design and Manufacturing of an MEMS device or a microsystem**.**

Course Outcome: By the end of the course, the students shall be able to

1. Understand working principles of currently available microsensors, actuators used in Microsystems.
2. Apply scaling laws that are used extensively in the conceptual design of micro devices and systems.
3. Understand the basic principles and applications of micro-fabrication processes.

UNIT I: **(8)**

Micro-fabrication and Micromachining : Integrated Circuit Processes, Bulk Micromachining : Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA)

UNIT II: **(8)**

Physical Microsensors: Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples: Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors

UNIT III: **(9)**

Microactuators: Electromagnetic and Thermal microactuation, Mechanical design of microactuators, Microactuator examples, microvalves, micropumps, micromotors-Microactuator systems : Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector

UNIT IV: **(10)**

Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micromachined Systems: Success Stories, Micromotors, Gear trains, Mechanisms.

UNIT V: **(9)**

Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays. MEMS for RF Applications: Need for RF MEMS components in communications, space and defense applications.

TEXT BOOKS:

1. Sensor Technology and Devices: Ristic L (ed), Artech House, London, 1994.
2. Semiconductor Sensors: Sze S.M. (ed), John Wiley, New York, 1994.
3. RF MEMS and Their Applications: Vijay Varadan, K. J. Vinoy, K. A. Jose, Wiley, 2002.

REFERENCE BOOKS :

1. Integrated Sensors, Micro actuators and micro-systems (MEMS): K.D. Wise, Special Issue of proceedings of IEEE, Vol. 86, No.8, August 1998
2. RF MEMS: Theory, Design, and Technology: Gabriel M. Rebeiz, Wiley, 2003.
3. Fundamentals of Microfabrication: Marc Madou, CRC Press, 1997.

Elective-III (Discipline Specific):

PGVLS204/3T	High Speed Semiconductor Devices and Circuits

Course Objectives:

1. To study crystal structure of Semiconductors.
2. To study different MOS devices and their characteristics.
3. To study Advanced Devices HBT and HEMT Devices
4. To study the fabrication process in detail.
5. To study different MOS Integration Techniques.

Course Outcome: By the end of the course the students shall be able to:

1. Identify different MOS devices for the specific application.
2. Fabrication of different MOS devices corresponding to the requirements.
3. Integrate different MOS devices.

UNIT I: Review of Crystal Structure: (9)

Crystal structure of important semiconductors (Si, GaAs, InP), electrons in periodic lattices, energy band diagram, carrier concentration and carrier transport phenomenon, electrical, optical, thermal and high field properties of semiconductors, Homojunction Devices, Homojunction Devices (BJT and FET): Structure, band diagram, operation, I–V and C–V characteristics (analytical expressions), small signal switching models.

UNIT II: MOS Devices: (9)

MOS Diode: Structure, band diagram, operation, C–V characteristics, effects of oxide charges, avalanche injection, high field effects and breakdown; Heterojunction Based MOSFET: Band diagram, structure, operation, I–V and C–V characteristics (analytical expressions), MOSFET breakdown and punch through, subthreshold current, scaling down; Alternate High k-dielectric Materials: HF–MOSFETs - SOI MOSFET - buried channel MOSFET - charge coupled devices.

UNIT III: Advanced Devices HBT and HEMT Devices: (8)

AlGaAs/ GaAs, InP and SiGe based HBT and HEMT structure, band diagram, operation, I–V and C–V characteristics (analytical expressions), small signal switching models, benefits of heterojunction transistor for high speed applications.

UNIT IV: (9)

Fabrication and Characterization Techniques Crystal Growth and Wafer Preparation: Epitaxy, diffusion, ion implantation, dielectric film deposition and oxidization techniques, masking and lithography techniques (optical, e-beam and other advanced lithography techniques), metallization

UNIT V: (9)

Bipolar and MOS integration techniques, interface passivation techniques; Characterization Techniques: Four probe and Hall Effect measurement, I–V and C–V for dopant profile characterization and DLTS.

TEXT BOOKS:

1. High Speed Semiconductor Devices , S.M.Sze, Willey, 1990
2. Nandita Das Gupta and Amitava Das Gupta, “Semiconductor Devices: Modeling and Technology”, Prentice Hall of India, 2004.

REFERENCE BOOKS:

1. M. S. Tyagi, “Introduction to Semiconductor Materials and Devices”, John Wiley and Sons, 2008.
2. J. Singh, “Semiconductor Devices: Basic Principles”, John Wiley and Sons, 2007.

Foundation-I

Laboratory-I:

PGVLS206P	Analog VLSI Design

Any EIGHT practicals are to be conducted based on the syllabus of Analog VLSI Design [PGVLS201T]

Laboratory-II:

PGVLS207P	Modeling of Digital System and Testing

Any EIGHT practicals are to be conducted based on the syllabus of Modeling of Digital System and Testing [PGVLS203T]

R.T.M. Nagpur University
Scheme of Examination for
M. Tech. (VLSI) Third Semester

Foundation-II